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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,012	07/15/2003	Stuart Ryan	SHI-003	9109

7590 02/28/2006

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,012	RYAN ET AL.	
	Examiner	Art Unit	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9,12-17 and 20-26* is/are rejected.

7)☒ Claim(s) *7,10,11,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6, 8-9,12-17, and 20-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Mitsuishi, US 6907514. The rejections are maintained.

As per claims 1, 12, and 26, Mitsuishi teaches an integrated circuit comprising: a processor operable to issue memory access requests (e.g., fig. 1, microcomputer 1, CPU 2, col. 12, lines 55-60) each memory access request identifying an address in memory to which the request is directed (e.g., col. 18, lines 23-45; col. 14, lines 5-65); at least one on-chip resource falling within the address space addressable by the processor (e.g., col. 18, lines 23-45; col. 14, lines 5-65); an interface for directing packets off-chip and addressable within the address space of the processor (e.g., fig. 1, controller 12,); and a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps (e.g., fig. 4, col. 18, lines 23-40), wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of

addresses allocated to said interface (e.g., fig. 4, col. 18, lines 23-40), and in said second memory address map said first range of addresses are also allocated to the interface (e.g., fig. 4, col. 18, lines 23-40); and an off chip circuit connected to said interface and including at least one off chip memory resource (e.g., fig. 9, 105, 103, 101)

As per claim 20, Mitsuishi teaches a method of evaluating a prototype system comprising an integrated circuit including an on-chip processor (e.g., fig. 1, CPU 2) associated with at least one on-chip memory resource (e.g., fig. 1, RAM 6, ROM 5) and an off-chip circuit associated with at least one off-chip memory resource (e.g., fig. 9, RAM 101), the method comprising: executing a computer program on the on-chip processor, said program causing the generation of memory access requests (e.g., col. 5, lines 48-55), each memory access request including an address identifying an address in memory to which the request is directed (e.g., col. 18, lines 23-30); and in accordance with a selected mode of operation, selectively supplying said memory access requests to at least one of said first and second memory address maps (e.g., col. 18, lines 23-45), and directing the memory access requests selectively to said on-chip memory resource or said off-chip circuit in dependence on the selected one of said first and second address maps (e.g., fig 4, MSROM, MSRAM or EXTA col. 18, lines 23-50).

As per claims 2, 8, 13, 21, Mitsuishi teaches an integrated circuit according to claim 1, which comprises a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map

is utilized (e.g., fig. 4, mode; col. 18, lines 23-40); wherein said mode is set by application of a logic value selected from one and zero on the mode setting pin (e.g., fig. 4, mode; col. 18, lines 23-40) .

As per claims 3, 4, 14, Mitsuishi teaches wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps (e.g., fig. 4, And gates and Mode); said switching means comprises a multiplexer (e.g., fig. 4, And gates and Mode).

As per claims 5, 15, Mitsuishi teaches wherein said at least one on-chip resource comprises a memory mapped peripheral (e.g., col. 18, lines 23-30).

As per claims 6, 16, Mitsuishi teaches wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource (e.g., fig. 1, RAM 5).

As per claims 9, 17, Mitsuishi teaches wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip (e.g., fig. 1, I/O ports).

As per claim 22, Mitsuishi teaches wherein said memory access requests are directed off-chip via an interface whose address space replaces the address space of the on-chip memory resource in the second memory address map (e.g., fig. 4, mode; col. 18, lines 23-40).

As per claims 23-25, Mitsuishi teaches wherein said memory access requests take the form of packets (e.g., col. 3, lines 30-35); wherein packets are chopped into chunks and transmitted in a plurality of cycles when being conveyed off-chip (e.g., col. 3, lines 30-35); wherein chunks received in a plurality of cycles from the off-chip circuit are reassembled into packets for transmission on-chip (e.g., col. 3, lines 30-35).

4. Claims 7, 10-11, and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Applicant's arguments filed 12/1/05 have been fully considered but they are not persuasive.

6. In the remarks, the applicant argued that nothing in Mitsuishi appears to teach the claimed limitations "a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated

to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface; and an off-chip circuit connected to said interface and including at least one off chip memory resource."

The examiner disagreed with the applicant's arguments. Mitsuishi teaches a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps (e.g., fig. 4, col. 18, lines 23-40), wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface (e.g., fig. 4, col. 18, lines 23-40), and in said second memory address map said first range of addresses are also allocated to the interface (e.g., fig. 4, col. 18, lines 23-40); and an off chip circuit connected to said interface and including at least one off chip memory resource (e.g., fig. 9, 105, 103, 101). According to, figs. 2, 4 and col. 18, lines 23-40, Mitsuishi shows selecting one of a first address map (i.e., address of an internal device, ROM5) and a second address map (i.e., address of an external space) wherein the first address map having a first range of addresses allocated to said at least one on chip resource (i.e., ROM 5 can be mapped to area 0 or 1 shown in figs. 2, fig. 4 H20000-H'207FF) and a second range of addresses allocated to said interface (i.e., EXTA to external controller 121) and in the second memory address map said first range of addresses are also allocated to said interface (i.e., area 0-7 for external address space; e.g., col. 14, lines 30-60 and fig. 2).

7. In the remarks, the applicant argued that Mitsuishi, col. 13, line 62 to col. 14, line 38 includes no teaching of "a first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface."

The examiner disagreed with the applicant's arguments. Mitsuishi, figs. 2-4, col. 13, line 62 to col. 14, line 38 and col. 18, lines 23-40 include teaching of "a first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface" as required in claim 1. In particular, col. 14, lines 6-10, teaches a first address map has a first range of address H'200000 to H'207FFF, area 0 or 1 allocated to an embedded ROM5 and col. 14, lines 30-60, teaches a second range of addresses allocated to an interface for directing packet off chip, (i.e. external interface 121, col. 18, lines 23-40), and col. 14, lines 30-60 and fig. 2, teaches second memory map where the first range of addresses are also allocated to the interface (i.e., an external space including area 0-7).

Also, Mitsuishi teaches a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps (e.g., fig. 4, col. 18, lines 23-40), wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface (e.g., fig. 4, col. 18, lines 23-40), and in said second memory address map said first range of addresses are also allocated to

the interface (e.g., fig. 4, col. 18, lines 23-40); and an off chip circuit connected to said interface and including at least one off chip memory resource (e.g., fig. 9, 105, 103, 101). According to, figs. 2, 4 and col. 18, lines 23-40, Mitsuishi shows selecting one of a first address map (i.e., address of an internal device, ROM5) and a second address map (i.e., address of an external space) wherein the first address map having a first range of addresses allocated to said at least one on chip resource (i.e., ROM 5 can be mapped to area 0 or 1 shown in figs. 2, fig. 4 H20000-H'207FF) and a second range of addresses allocated to said interface (i.e., EXTA to external controller 121) and in the second memory address map said first range of addresses are also allocated to said interface (i.e., area 0-7 for external address space; e.g., col. 14, lines 30-60 and fig. 2).

8. In the remarks, the applicant argued that Mode selector in fig. 4, of Mitsuishi does not appear to function as means for selectively supplying memory access requests to at least one of the first and second memory address maps.

The examiner disagreed with the applicant's arguments. According to fig.4, Mitsuishi teaches either a memory access requests to a first range or a second range of addresses will be selected based on a value of MODE. Also depends on the values of the MODE either a Rom address map or external address map will be selected. In addition, col. 18, lines 23-40, Mitsuishi teaches a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps (e.g., fig. 4, col. 18, lines 23-40).

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Denise Tran

2/20/06